REMARKS

In the final Office Action, the Examiner notes that claims 1, 3-9 are allowed and 10, 12-14 and 16 are pending and rejected. By this response, Applicant has herein amended claim 10. Clam 16 is hereby cancelled.

In view of both the amendments presented above and the following discussion, Applicant submits that none of the claims now pending in the application are obvious under the provisions of 35 U.S.C. §103. Thus, Applicant believes that all of the pending claims are now allowable.

It is to be understood that Applicant, by amending the claims, does not acquiesce to the Examiner's characterizations of the art of record or to Applicant's subject matter recited in the pending claims. Further, Applicant is not acquiescing to the Examiner's statements as to the applicability of the art of record to the pending claims by filing the instant responsive amendments.

The Applicant's Representative thanks the Examiner for taking the time to review and consider the proposed claim amendment provided by Applicant's Representative. The Applicant's Representative also thanks the Examiner for agreeing to enter the proposed amended after the final Office Action mailed on November 21, 2005.

REJECTIONS

35 U.S.C. § 103(a)

Claims 10, 12-14 and 16

The Examiner rejected claims 10, 12-14 and 16 under 35 U.S.C. §103(a) as being unpatentable over the instant application's disclosed prior art in view of Balakrishnan et al. (US 6,611,567, hereinafter "Balakrishnan"). The rejection is respectfully traversed.

Applicant's disclosed prior art discloses an encoder, including a differential encoder, a constellation mapper, and in-phase and quadrature filters. Applicant's disclosed prior art, however, fails to teach or suggest Applicant's invention as a whole. Namely, as acknowledged by the Examiner, Applicant's disclosed prior

art fails to teach or suggest at least the claimed limitations of "wherein each VAS comprises a plurality of vector registers (VR) for storing precomputed pulse shaping values and a vector arithmetic unit (VAU) for arithmetically processing a selected vector and an accumulated vector, said selected vector comprising a plurality of pre-computed values selected from said vector registers in response to a received component signal."

Furthermore, Balakrishnan fails to bridge the substantial gap as between Applicant's disclosed prior art and Applicant's invention of at least claim 10. In general, Balakrishnan discloses a method and apparatus for pulse shaping. As taught in Balakrishnan, a set of bits representing a symbol is received and a corresponding output value is generated by adding or subtracting a received coefficient and a received value based on a predetermined one of the set of bits.

Balakrishnan, however, fails to teach or suggest Applicant's invention as a whole. Namely, Balakrishnan fails to teach or suggest at least the limitations of "shaping, using a pair of respective vector arithmetic structures, said in-phase component and said quadrature component to produce respective shaped in-phase and quadrature components, wherein, for each of said in-phase component and said quadrature component, said shaping comprises arithmetically processing a selected vector and an accumulated vector in response to receiving said respective component, said selected vector comprising a plurality of pre-computed pulse shaping values selected from a plurality of vector registers to impart a desired shape to said respective component," as taught in Applicant's invention of at least claim 10.

Rather, Balakrishnan discloses that only one value may be processed at a time. In particular, Balakrishnan specifically teaches the use of switches for switching between processing of real and imaginary values. (Balakrishnan, FIGs. 6, 7, 11). In particular, with respect to FIG. 6, Balakrishnan specifically states that "a first switch 16 receives the output of the add/subtract block 14, and supplies the output of the add/subtract block 14 to either the real or imaginary output of the QPSK processing block QPB...." (Balakrishnan, Col. 4 Line 66 –

Col. 5 Line 2; Emphasis added). Similarly, with respect to FIG. 7, Balakrishnan specifically states that "[t]he second switch 24 supplies one of the real and imaginary outputs to the add/subtract block 14, based on the value of the second bit b_1...when the second bit b_1 is 0, the [second] switch 24 supplies the real value...and when the second bit b_1 is 1, the [second] switch 24 supplies the imaginary value...." (Balakrishnan, Col. 6 Lines 13 -63).

In other words, Balakrishnan teaches that a real value is processed and output if the switch is set in the R-position, while, alternatively, an imaginary value is processed and output if the switch is set in the I-position. For example, with respect to FIG. 11 of Balakrishnan referenced by the Examiner in the Office Action, when switches 24 and 16 are set in the R-position, only the real value is processed and switch 28 is set in the I-position for enabling the imaginary value to pass through unprocessed. Similarly, with respect to FIG. 11 of Balakrishnan referenced by the Examiner in the Office Action, when switches 24 and 16 are set in the I-position, the imaginary value is processed and switch 28 is set in the R-position for enabling the real value to pass through unprocessed.

In other words, as taught in Balakrishnan, the switches 24 and 16 used for choosing between processing a real value or an imaginary value may only be set in one position or another. Furthermore, switch 28 used for choosing the value to be passed through without any processing is set in a position opposite of the settings of switches 24 and 16 (i.e., when switches 24 and 16 are set to the R-position switch 28 is set to the I-position, and vice versa). As such, as taught in Balakrishnan, real and imaginary values simply cannot be processed in parallel. Thus, the teachings of Balakrishnan are completely different from Applicant's invention of at least claim 10.

Furthermore, since only one value at a time (either a real value or an imaginary value) may be processed in the Balakrishnan system, Balakrishnan teaches a single coefficient register (illustratively, COEF REG 126 depicted in FIG. 7 of Balakrishnan). Thus, when a switch that alternates between processing of real and imaginary values is set in the R-position, the coefficient register

provides coefficients for shaping the real value. Similarly, when a switch that alternates between processing of real and imaginary values is set in the I-position, the coefficient register provides coefficients for shaping the imaginary value. Thus, Balakrishnan uses a single coefficient register for alternating processing of real and imaginary values.

In Applicant's invention of at least claim 10, on the other hand, the in-phase VAS comprises a plurality of vector registers for storing precomputed pulse shaping values for shaping the in-phase component. Similarly, in Applicant's invention of at least claim 10, the quadrature VAS comprises a plurality of vector registers for storing pre-computed pulse shaping values for shaping the quadrature component. In other words, as taught in Applicant's invention of at least claim 10, distinct sets of vector registers provide pulse shaping coefficients for the in-phase VAS and the quadrature VAS, respectively. A single coefficient register for serially shaping real and imaginary values, as taught in Balakrishnan, is simply not a first plurality of vector registers having coefficients for shaping in-phase components and a second plurality of vector registers having coefficients for shaping quadrature components such that the in-phase and quadrature pulse shaping is performed in parallel, as taught in Applicant's invention of at least claim 10.

The teachings of Balakrishnan are completely different from Applicant's invention of at least claim 10. Thus, the design and operation of the Balakrishnan system is completely different from the design and operation of Applicant's invention of claim 10. As such, Balakrishnan fails to teach or even suggest at least Applicant's claimed limitations of "shaping, using a pair of respective vector arithmetic structures, said in-phase component and said quadrature component to produce respective shaped in-phase and quadrature components, wherein, for each of said in-phase component and said quadrature component, said shaping comprises arithmetically processing a selected vector and an accumulated vector in response to receiving said respective component, said selected vector comprising a plurality of pre-computed pulse shaping values selected from a

plurality of vector registers to impart a desired shape to said respective component." Therefore, Balakrishnan fails to teach or suggest Applicant's invention as a whole.

The test under 35 U.S.C. §103 is not whether an improvement or a use set forth in a patent would have been obvious or non-obvious; rather the test is whether the claimed invention, considered as a whole, would have been obvious. Jones v. Hardy, 110 USPQ 1021, 1024 (Fed. Cir. 1984) (emphasis added). Moreover, the invention as a whole is not restricted to the specific subject matter claimed, but also embraces its properties and the problem it solves. In re Wright, 6 USPQ 2d 1959, 1961 (Fed. Cir. 1988) (emphasis added). Balakrishnan, alone or in combination with Applicant's disclosed prior art, fails to teach or suggest Applicant's invention as a whole.

Furthermore, Applicant's disclosed prior art and Balakrishnan cannot be operatively combined. Applicant's disclosed prior art discloses parallel filters for processing the in-phase and quadrature signal components in parallel. As described herein, however, Balakrishnan performs serial processing on real and imaginary values using a plurality of switches for alternating between the real and imaginary values. As taught in Balakrishnan, if a real value is selected for processing, the imaginary value passes through unprocessed, and, alternatively, if an imaginary value is selected for processing, the real value passes through unprocessed. Therefore, the parallel processing functions of Applicant's disclosed prior art simply cannot be operatively combined with the serial processing functions of Balakrishnan.

As such, Applicant submits that independent claim 10 is non-obvious over Applicant's disclosed prior art in view of Balakrishnan and is patentable under 35 U.S.C. §103(a). Furthermore, claims 12-14 and 16 depend, either directly or indirectly, from independent claim 10 and recite additional features thereof. As such, and for at least the same reasons discussed above, Applicant submits that these dependent claims are also non-obvious over Applicant's disclosed prior art

in view of Balakrishnan and are patentable under 35 U.S.C. §103. Therefore, Applicant respectfully requests that the rejections be withdrawn.

ALLOWABLE SUBJECT MATTER

Applicant thanks the Examiner for the allowance of claims 1 and 3-9.

SECONDARY REFERENCES

The secondary references made of record are noted. However, it is believed that the secondary references are no more pertinent to Applicant's disclosure than the primary references cited in the Office Action. Therefore, Applicant believes that a detailed discussion of the secondary references is not necessary for a full and complete response to this Office Action.

CONCLUSION

Thus, Applicant submits that none of the claims presently in the application are obvious under the provisions of 35 U.S.C. §103. Consequently, Applicant believes that all of these claims are presently in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issue are earnestly solicited.

If however, the Examiner believes that there are any unresolved issues requiring adverse final action in any of the claims now pending in the application, it is requested that the Examiner telephone Michael Bentley at (732) 383-1434 or Eamon J. Wall, Esq. at (732) 530-9404 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

Respectfully submitted,

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E J Wall

Eamon J. Wall, Attorney
Reg. No. 39,414

PATTERSON & SHERIDAN, LLP
595 Shrewsbury Avenue, Suite 100
Shrewsbury, New Jersey 07702
732-530-9404 - Telephone
732-530-9808 – Facsimile